High-Speed Circuit Lab (博理 404)

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• BS 1992 EE NTU
• MS 1994 Stanford
• 1994 -1997 LSI Logic
• PhD 2001 UCLA

Course
• Electronic Circuits (III), (I)
• Analog Circuit Design
• Advanced Analog Circuit Design
• RF Circuit Design

Equipment
• Work Station : SunBlade2000/2500, IBM Linux Workstation, Sun Blade150
• PC : for every one (You can get extra one if you need one, such as P-3.4G …)
• Digital communication system
Why Mixed-signal Circuits-(II)?
Research Activities-(I)

● ADC ($$$$$):
  (1) High-resolution with digital calibration.
  (2) Low-to-medium resolution but very high speed (> few GHz)
  「類比電路數位化」(相同，數位電路類比化)的趨勢下，
  → Digital-Aided Calibrated Analog Circuit

● PLL System ($$$):
  (1) RF frequency synthesizer: 2.4-GHz/5-GHz or more
  (2) PLL architecture in RF frequency synthesizer: adaptive and distributed PFD architecture.

● Other mixed-signal blocks ($$):
  (1) CDR (clock and data recovery circuit)
  (2) Equalizer (Multiple level with architecture-level innovation)
  (3) TFT IC design
  (4) Batteryless IC design

Note: $ is proportional to complexity of the circuitry.
Research Activities-(II)

- Electrical/Electronic Engineering:
  \[ \rightarrow \textit{Engineering but not science !!!} \]

- 測不準原理
  \[ \rightarrow (\text{速度}) \times (\text{準度}) = \text{定值} \]

- Advanced technologies can improve constant. But, why bothers?

- Design innovation is the key value of a IC designer/researcher.
Analog Circuit is Art

(1) Design is art but not brute force.
→ Driving a Ferrari at 300+ km/h at high-way is nothing. But, driving a normal car at 300+km/h requires significant hard work.

(2) The mission of our lab:
→ Combine circuit/architecture innovation with advanced technology to create state-of-the-art design.

(3) Extend yourself in multi-discipline world:
   (IC = Indian + Chinese, where do Taiwanese go???)
→ Broad vision is very important for all of you.
What you are going to learn here

(1) System-level design: FIR vs. IIR, discrete-time vs. continuous-time

(2) Circuit design: passive delay line or active delay line

(3) Physical design: how to produce very symmetric device

(4) Board-level design: impedance matching, on-chip coupling.

(5) Measurement equipment setup.
Lab Achievement

(1) Alumni: Except military service/PhD, half of our MS alumni work at Mediatek

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<th>Year</th>
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<tbody>
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<td>2006</td>
<td>陳坵褫</td>
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<tr>
<td>2004</td>
<td>曹盛煌</td>
<td>瑞昱</td>
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<tr>
<td>2004</td>
<td>呂嘉祥</td>
<td>百力達科技公司</td>
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<tr>
<td>2005</td>
<td>廖英閔</td>
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<td>2005</td>
<td>李韋良</td>
<td>MTK</td>
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<td>2005</td>
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<td>2005</td>
<td>王維德</td>
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(2) Publications: First-tier conference and journal such as ISSCC and Journal of Solid-State Circuits.

(3) Awards: 3-time 教育部 IC design contest 特優, 2-time MXIC (旺宏電子) 金矽獎及其他

Welcome to join
High-Speed Circuit Lab!